Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A data transfer control device for data transfer through a bus, comprising:

a circuit ~~which~~ that is ~~connected~~ connectable to a first bus, the first bus being connectable to a first device;

an interface circuit ~~which~~ that is connectable to a second bus and is coupled to the circuit, the second bus being connectable to a second device;

a non-volatile memory ~~which~~ that stores at least one of device information and data transfer control program information and is coupled to the circuit; and

a processor that is coupled to the interface circuit,

the processor including:

a rewriter; and

a rewriter activation section,

the data transfer control device having a bus bridge function between the first bus conforming to a first interface standard and the second bus conforming to a second interface standard, the bus bridge function being realized by issuing a command included in ~~the~~ a command packet transferred from the first device through the first bus, to the second device through the second bus,

the rewriter activation section automatically activating the rewriter to start processing when the second bus is detected to have no connection to any device before a normal data transfer using the bus bridge function,

the rewriter loading and writing information transferred from the first device through the first bus into a rewrite area of the non-volatile memory when the rewriter is activated by the rewriter activation section,

when the second bus is detected to have a connection to the second device, the circuit performing packet transfer through the first bus conforming to the first interface standard and the interface circuit performing interface processing with the second device conforming to the second interface standard to realize the normal data transfer using the bus bridge function,

the non-volatile memory having an area in which is stored information for indicating whether or not the data transfer control program information has been written correctly into the rewrite area.

2. (Previously Presented) The data transfer control device as defined in claim 1,

wherein the detection of whether or not the second bus is connected to the second device is based on the result of an access to a register of the second device.

3. (Previously Presented) The data transfer control device as defined in claim 1,

wherein the rewriter writes information into the rewrite area by performing data transfer between the data transfer control device and the first device connected to the first bus in a mode of loading information to the rewrite area.

4. (Previously Presented) The data transfer control device as defined in claim 1,

wherein data transferred from the first device through the first bus is transferred to the second device through the second bus, and data transferred from the second device through the second bus is transferred to the first device through the first bus, in an ordinary operating mode that differs from a mode of loading information to the rewrite area.

5. (Original) The data transfer control device as defined in claim 1,

wherein the device information includes identification information that is specific to an electronic instrument in which the data transfer control device is embedded.

6. (Canceled)

7. (Currently Amended) ~~The data transfer control device as defined in claim 1, wherein:~~A data transfer control device for data transfer through a bus, comprising:

a circuit that is connectable to a first bus, the first bus being connectable to a first device;

an interface circuit that is connectable to a second bus and is coupled to the circuit, the second bus being connectable to a second device;

a non-volatile memory that stores at least one of device information and data transfer control program information and is coupled to the circuit; and

a processor that is coupled to the interface circuit,

the processor including:

a rewriter; and

a rewriter activation section;

that data transfer control device having a bus bridge function between the first bus conforming to a first interface standard and the second bus conforming to a second interface standard, the bus bridge function being realized by issuing a command included in a command packet transferred from the first device through the first bus, to the second device through the second bus,

the rewriter activation section automatically activating the rewriter to start processing when the second bus is detected to have no connection to any device before a normal data transfer using the bus bridge function,

the rewriter loading and writing information transferred from the first device through the first bus into a rewrite area of the non-volatile memory when the rewriter is activated by the rewriter activation section,

when the second bus is detected to have a connection to the second device, the circuit performing packet transfer through the first bus conforming to the first interface standard and the interface circuit performing interface processing with the second device conforming to the second interface standard to realize the normal data transfer using the bus bridge function,

the non-volatile memory ~~has~~ having an area in which is stored rewriter processing setting information for setting whether processing by the rewriter is enabled or disabled; and

the rewriter processing setting information ~~is~~ being set to be enabled in an initial state but ~~is~~ being set to be disabled at the end of processing by the rewriter.

8. (Canceled)

9. (Currently Amended) An electronic instrument comprising:

a data transfer control device including

a circuit ~~which~~ that is ~~connected~~ connectable to a first bus, the first bus being connectable to a first device;

an interface circuit ~~which~~ that is connectable to a second bus and is coupled to the circuit, the second bus being connectable to a second device;

a non-volatile memory ~~which~~ that stores at least one of device information and data transfer control program information and is coupled to the circuit; and

a processor that is coupled to the interface circuit,

the processor including:

a rewriter; and

a rewriter activation section, and

the second device connected to the second bus;

the data transfer control device having a bus bridge function between the first bus conforming to a first interface standard and the second bus conforming to a second interface standard, the bus bridge function being realized by issuing a command included in ~~the~~ a command packet transferred from the first device through the first bus, to the second device through the second bus,

the rewriter activation section automatically activating the rewriter to start processing when the second bus is detected to have no connection to any device before a normal data transfer using the bus bridge function,

the rewriter loading and writing information transferred from the first device through the first bus into a rewrite area of the non-volatile memory when the rewriter is activated by the rewriter activation section,

when the second bus is detected to have a connection to the second device, the circuit performing packet transfer through the first bus conforming to the first interface standard and the interface circuit performing interface processing with the second device conforming to the second interface standard to realize the normal data transfer using the bus bridge function,

the non-volatile memory having an area in which is stored information for indiating whether or not the data transfer control program information has been written correctly into the rewrite area.

10-14. (Canceled)

15. (New) An electronic instrument comprising:

a data transfer control device including

a circuit that is connectable to a first bus, the first bus being connectable to a first device;

an interface circuit that is connectable to a second bus and is coupled to the circuit, the second bus being connectable to a second device;

a non-volatile memory that stores at least one of device information and data transfer control program information and is coupled to the circuit; and

a processor that is coupled to the interface circuit,

the processor including:

a rewriter; and

a rewriter activation section, and

the second device connected to the second bus;

that data transfer control device having a bus bridge function between the first bus conforming to a first interface standard and the second bus conforming to a second interface standard, the bus bridge function being realized by issuing a command included in a command packet transferred from the first device through the first bus, to the second device through the second bus,

the rewriter activation section automatically activating the rewriter to start processing when the second bus is detected to have no connection to any device before a normal data transfer using the bus bridge function,

the rewriter loading and writing information transferred from the first device through the first bus into a rewrite area of the non-volatile memory when the rewriter is activated by the rewriter activation section,

when the second bus is detected to have a connection to the second device, the circuit performing packet transfer through the first bus conforming to the first interface standard and the interface circuit performing interface processing with the second device

conforming to the second interface standard to realize the normal data transfer using the bus bridge information,

the non-volatile memory having an area in which is stored rewriter processing setting information for setting whether processing by the rewriter is enabled or disabled; and

the rewriter processing setting information being set to be enabled in an initial state but being set to be disabled at the end of processing by the rewriter.